IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently amended) A circuit operation verifying method for verifying that each of a number of circuit elements of a semiconductor circuit in layout design satisfies specifications, the method comprising the steps of:

loading condition information of the semiconductor circuit as electrical specifications on voltages and currents applied to the circuit elements, circuit diagram data representing connection information of the semiconductor circuit, and input patterns of voltages and currents used for circuit operation simulation with respect to time;

simulating operation of the semiconductor circuit by computing voltage values or current values with respect to time of the circuit elements of the semiconductor circuit based on the loaded circuit diagram data and input patterns, said simulating operation being performed at each of a plurality of specific times which are incrementally increasing, and storing the computed values in a memory after each simulating operation;

verifying that the circuit elements of the semiconductor circuit satisfy the loaded condition information using the voltage values or the current values of the circuit elements stored in the memory, said verifying step being performed after each simulating operation; and

calculating a next specific time used for a next simulating step and a next verification step by adding an infinitesimal time to the specific time after the verifying step,

wherein the simulating step, the verifying step and the calculating step are performed repeatedly, and

wherein a low-precision, high-speed operation simulation is executed for the semiconductor circuit using the input patterns, to prepare operation information on the circuit elements of the semiconductor circuit and circuit hierarchical information on the semiconductor circuit.

2. (Cancelled)

3. (Previously presented) The method of Claim 1, wherein the condition information includes time specifications representing the frequency of violation against the electrical specifications or the time period for which a violation state is allowable, and

whether or not the frequency of violation or the violation allowable time period of each of the circuit elements of the semiconductor circuit satisfy the time specifications being determined using the voltage values or the current values with respect to time of the circuit element stored in the memory.

4. (Currently amended) The method of Claim 1, wherein upon termination of the simulating step and the verification step, results of [[the]] condition verification are displayed on a waveform display apparatus displaying results of the operation simulation or a design apparatus used for circuit design or layout design of the semiconductor circuit.

5. (Previously presented) The method of Claim 1, wherein a verification period during which a condition verification is to be executed for the semiconductor circuit or a non-verification period during which no condition verification is to be executed is designated; and

the condition verification for the semiconductor circuit is executed during the verification period.

6. (Previously presented) The method of Claim 1, wherein the specifications in the condition information are commonly designated for all the circuit elements of the semiconductor circuit, or individually designated for the respective circuit elements.

7. (Currently amended) A circuit operation verifying method for verifying that each of a number of circuit elements of a semiconductor circuit in layout design satisfies specifications, the method comprising the steps of:

loading condition information of the semiconductor circuit as electrical specifications on voltages and currents applied to the circuit elements, circuit diagram data representing connection information of the semiconductor circuit, and input patterns of voltages and currents used for circuit operation simulation with respect to time;

simulating operation of the semiconductor circuit while computing voltage values or current values with respect to time of the circuit elements of the semiconductor circuit based on the loaded circuit diagram data and input patterns and storing the computed values in a memory; and

verifying that the circuit elements of the semiconductor circuit satisfy the loaded condition information using the voltage values or the current values of the circuit elements stored in the memory, said verifying step being performed concurrently with said simulating operation,

wherein the specifications in the condition information are commonly designated for all the circuit elements of the semiconductor circuit, or individually designated for the respective circuit elements,

wherein a low-precision, high-speed operation simulation is executed for the semiconductor circuit using the input patterns, to prepare operation information on the circuit elements of the semiconductor circuit and circuit hierarchical information on the semiconductor circuit, [[;]]

wherein a plurality of circuit portions, each having an operation pattern and a hierarchical state, in the semiconductor circuit are retrieved based on the operation information, the circuit hierarchical information, and the circuit diagram data, and

wherein the specifications in the condition information are individually designated for only one circuit portion among the retrieved plurality of circuit portions so that a condition verification is executed for only circuit elements included in the one circuit portion.

8. (Currently amended) The method of Claim 1, ~~wherein a low-precision, high-speed operation simulation is executed for the semiconductor circuit using the input patterns, to prepare operation information on the circuit elements of the semiconductor circuit and circuit hierarchical information on the semiconductor circuit;~~

wherein a plurality of circuit portions, each having an operation pattern and a hierarchical state, in the semiconductor circuit are retrieved based on the operation information, the circuit hierarchical information, and the loaded circuit diagram data, [[;]] and

wherein the retrieved plurality of circuit portions are united into one circuit portion, to reduce the circuit diagram data.

9. (Currently amended) A circuit operation verifying apparatus for verifying that each of a number of circuit elements of a semiconductor circuit in layout design satisfies specifications, the apparatus comprising:

loading means for loading condition information of the semiconductor circuit as electrical specifications on voltages and currents applied to the circuit elements, circuit diagram data representing connection information of the semiconductor circuit, and input patterns of voltages and currents used for circuit operation simulation with respect to time;

operation simulation means for simulating operation of the semiconductor circuit by computing voltage values or current values with respect to time of the circuit elements of the semiconductor circuit based on the circuit diagram data and the input patterns loaded by the loading means, said simulating operation being performed at each of a plurality of specific times which are incrementally increasing, and storing the computed voltage values or current values in a memory after each simulating operation;

verification means for verifying that the circuit elements of the semiconductor circuit satisfy the specifications in the loaded condition information using the voltage values or the current values of the circuit elements stored in the memory; and

calculating means for calculating a next specific time used for the operation simulating means and the verification means by adding an infinitesimal time to the specific time after the verification means performs said verification,

wherein the operation simulating means, the verifying means and the calculating means are performed repeatedly, and

wherein a low-precision, high-speed operation simulation is executed for the semiconductor circuit using the input patterns, to prepare operation information on the circuit elements of the semiconductor circuit and circuit hierarchical information on the semiconductor circuit.

10. (Currently amended) A circuit operation verifying apparatus for verifying that each of a number of circuit elements of a semiconductor circuit in layout design satisfies specifications, the apparatus comprising:

loading means for loading condition information as electrical specifications on voltages and currents applied to the circuit elements, circuit diagram data representing connection information of the semiconductor circuit, and input patterns of voltages and currents used for circuit operation simulation with respect to time;

operation simulation means for simulating operation of the semiconductor circuit while computing voltage values or current values with respect to time of the circuit elements of the semiconductor circuit based on the circuit diagram data and the input patterns loaded by the loading means and storing the computed voltage values or current values in a memory;

verification means for verifying that the circuit elements of the semiconductor circuit satisfy the specifications in the loaded condition information using the voltage values or the current values of the circuit elements stored in the memory, said verification means performing said verification concurrently with said operation simulation means performing said simulating operation,

waveform display means for displaying results of the operation simulation of the semiconductor circuit performed by the operation simulation means; and

design means used for circuit design or layout design of a semiconductor circuit,

wherein verification results determined by the verification means are displayed on the waveform display means or the design means, and

wherein a low-precision, high-speed operation simulation is executed for the semiconductor circuit using the input patterns, to prepare operation information on the circuit elements of the semiconductor circuit and circuit hierarchical information on the semiconductor circuit.

11. (Currently amended) A circuit operation verifying method for verifying that each of a number of circuit elements of a semiconductor circuit in layout design satisfies specifications, the method comprising the steps of:

loading condition information of the semiconductor circuit as electrical specifications on voltages and currents applied to the circuit elements, circuit diagram data representing connection information of the semiconductor circuit, and input patterns of voltages and currents used for circuit operation simulation with respect to time;

simulating operation of the semiconductor circuit at a plurality of specific times by computing voltage values or current values with respect to time of the circuit elements of the semiconductor circuit based on the loaded circuit diagram data and input patterns, said simulating operation being performed at each of said plurality of specific times;

storing the computed values, which are the result of the simulation step, in a memory after each simulating operation;

verifying that the circuit elements of the semiconductor circuit satisfy the loaded condition information at each specific time using the voltage values or the current values of the circuit elements stored in the memory after each simulating operation; and

calculating a next specific time used for a next simulating step and a next verification step by adding an infinitesimal time to the specific time after the verifying step,

wherein the simulating step, the verifying step and the calculating step are performed repeatedly, and

wherein a low-precision, high-speed operation simulation is executed for the semiconductor circuit using the input patterns, to prepare operation information on the circuit elements of the semiconductor circuit and circuit hierarchical information on the semiconductor circuit.

12. (Previously presented) The method of Claim 11, wherein the condition information includes electrical specifications representing current density values and heat generation amounts of the circuit elements, the circuit diagram data of the semiconductor circuit includes layout information, and

current density analysis and heat generation analysis at positions inside the semiconductor circuit are performed based on the current values of the circuit elements and the layout information stored in the memory.